6. (AMENDED) The semiconductor integrated circuit as claimed in claim 1, wherein said wire dummies further avoid areas that are directly above positions of polysilicon or diffusion layers.

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8. (TWICE AMENDED) A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

B3

square dummy patterns provided in said wire layer and having different sizes,

wherein said square dummy patterns having different sizes are arranged at respective different pattern intervals.